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APPLICATION NUMBER: *60/529,340*
FILING DATE: *December 12, 2003*
RELATED PCT APPLICATION NUMBER: *PCT/US04/41243*

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EU352262929US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Zheng	Shen	Ann Arbor, MI

Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (500 characters max)

Mosfet Pair For Synchronous Rectification Forward Converters

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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OR

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City		State		Zip	
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ENCLOSED APPLICATION PARTS *(check all that apply)*

☑ Specification *Number of Pages* 6 ☐ CD(s), Number _____

☑ Drawing(s) *Number of Sheets* 14 ☑ Other (specify) Return Receipt Postcard Certificate of Express Mailing

☐ Application Date Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☑ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

☑ The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 06-0923

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE Amount ($): $80.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☑ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE _____

TYPED or PRINTED NAME William Hwang

TELEPHONE 973-992-1990

Date 12/12/2003

REGISTRATION NO. 36,169 *(if appropriate)*

Docket Number: 104023-666-PRO

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Mail Stop Provisional Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application No.	:	not yet assigned
Filing Date	:	not yet assigned
First Named Inventor	:	Zheng Shen
Attorney Docket No.	:	104023-666-PRO
Title	:	MOSFET PAIR FOR SYNCHRONOUS RECTIFICATION FORWARD CONVERTERS

CERTIFICATE OF EXPRESS MAILING

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Submitted herewith are the following items:

1) Provisional Application for Patent Cover Sheet (1 page);
2) Specification (6 pages);
3) Drawings with duplicate color copy (14 pages);
4) Certificate of Express Mailing (1 page); and
5) Return Receipt Postcard

Total Pages 22 pages plus postcard

Yvette Alvarez-Perez

CERTIFICATE OF EXPRESS MAILING

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Yvette Alvarez-Perez

December 12, 2003
Date

U.S. Provisional Patent Application Entitled

MOSFET PAIR FOR SYNCHRONOUS RECTIFICATION FORWARD CONVERTERS

Inventor(s):

Zheng Shen, Ann Arbor, MI

TITLE

[0001] MOSFET Pair For Synchronous Rectification Forward Converters

FIELD OF THE INVENTION

[0002] This invention generally relates to MOSFET pairs for self-driven or IC-driven synchronous rectification forward converters.

BACKGROUND OF THE INVENTION

[0003] As the operating voltage of microprocessors approaches the one-volt mark, operating currents continue to increase. Today's high-end notebook computers consume 20A. Servers and high-end desktop computers presently require 60 to 90A. The next-generation GHz class of microprocessors will require current as high as 130A. These changes in operating conditions challenge power components to maintain acceptable converter efficiency levels.

[0004] Isolated forward converters with a pair of synchronous rectification MOSFETs on the secondary is a common DC/DC topology for computer, telecom and networking industry. Either self- or IC-driven methods can be used to drive the secondary stage MOSFETs. Synchronous rectification is necessary to reduce power dissipation and maintain required efficiency. Examples of these are shown in Figure 1.

[0005] Referring now to Figure 2, in particular Figure 2a, there is shown during the conduction period (on-time) of the primary-side switch MOSFET (M1) (See Figure 1), the catch MOSFET (M3) is off and the current flows from the transformer to the inductor, output capacitor, and load, and then returns through the forward MOSFET (M2) to the transformer.

[0006] Figure 2b shows that as M1 turns off, the transformer current goes to zero. The load current is carried through M3 body diode momentarily, and then the transformer magnetizing current turns on M3 to allow reduced forward voltage drop. This also allows the transformer to reset, keeping volt-second balance on the transformer core.

[0007] M1 is the primary-side control switch while M2 and M3 are the secondary-side forward and catch (or freewheeling) synchronous MOSFETs respectively.

[0008] M1, M2, and M3 are currently discrete trench MOSFETs. For example, International Rectifier's 30V-rated IRF7822 or IRF6603 (DirectFETTM) are widely used for synchronous rectification applications.

[0009] The on-resistance and gate charge of the power MOSFETs have a great influence on the efficiency and compactness of DC/DC converters. Both low device on-resistance and low gate charge are necessary to run high-frequency DC-DC converters at a lower temperature or increase power density in the same form-factor. While trench MOSFETs exhibit very low specific on-resistance, they have a high gate charge due to the inherent vertical device structures.

[0010] It is also desirable to integrate M2 and M3 into a monolithic single device, and greatly reduce parts count, PCB space, and interconnect parasitics. However, this is not possible with the conventional trench power MOSFET technology.

[0011] On the other hand, lateral power MOSFETs, that until now are exclusively used in power ICs and as discrete RF devices, offer very low gate charge and reasonably low on-resistance. However, the use of lateral power MOSFETs is limited to small chip sizes and current ratings due to high metal interconnect parasitic resistance.

OBJECT OF THE INVENTION

[0012] It is one object of this invention is to provide a monolithic single power MOSFET pair with 3 or 5 terminals to replace the two secondary-side synchronous MOSFETs (catch and forward) for isolated forward DC/DC converters.

[0013] Another object is that the novel MOSFET pair should have a much lower gate charge, similar on-resistance, much lower gate resistance, much less interconnect parasitics, and much faster transition between the catch and forward MOSFETs than the prior art discrete circuit implementation.

[0014] It is yet another objective of this invention to provide a novel monolithic MOSFET pair in chip-scale packages for small PCB footprint, low package profile, low interconnect impedance, and junction-side cooling capability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The figures below depict various aspects and features of the present invention in accordance with the teachings herein.

DESCRIPTION OF THE INVENTION

[0016] The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling

within the scope of the present invention as defined herein and equivalents thereto. Use of absolute terms, such as "will not," "will," "shall," "shall not," "must," and "must not," are not meant to limit the present invention as the embodiments disclosed herein are merely exemplary.

[0017] Referring to Figure 3, there is shown in Figure 3a a 3 lead device for self-driven synchronous rectification topology: D1, D2, and common source (CS). There is also shown in Figure 5b a 5 lead device for control IC-driven synchronous rectification topology: D1, D2, G1, G2, and CS.

[0018] Figure 4 shows monolithic integration of the common-source catch and forward synchronous MOSFETs is made possible by adopting lateral LDMOS structure.

[0019] Figures 4a and 4b shows a first and second embodiments of interleaved D1/CS and D2/CS cell fingers.

[0020] Figure 5 shows additional embodiments with separate D1/CS and D2/CS cell sections made possible by adopting lateral LDMOS structure.

[0021] Figure 6 shows that 2, 3, or more metal-layer interconnects are combined with wafer bumping technique to reduce the metal parasitic resistance and offer a very low on-resistance even for large chip sizes. (This is further described in a separate patent application filed on June 15, 2003).

[0022] Figure 7 shows companies with potential applications and companies with prior art products.

CONCLUSION

[0023] Having now described preferred embodiments of the invention, it should be apparent to those skilled in the art that the foregoing is illustrative only and not

limiting, having been presented by way of example only. All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined by the appended claims and equivalents thereto.

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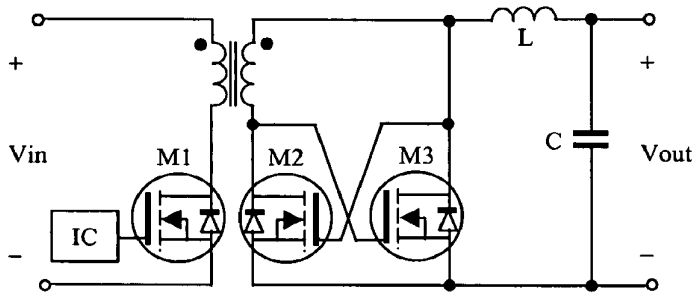
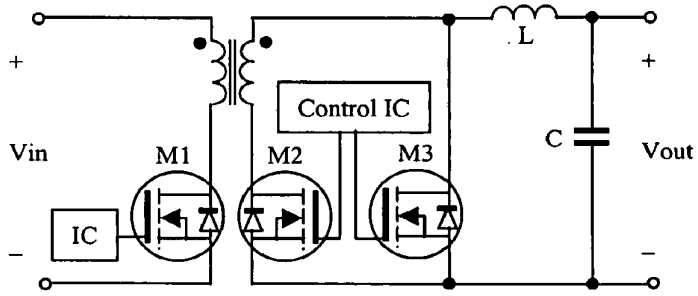
Figure 1

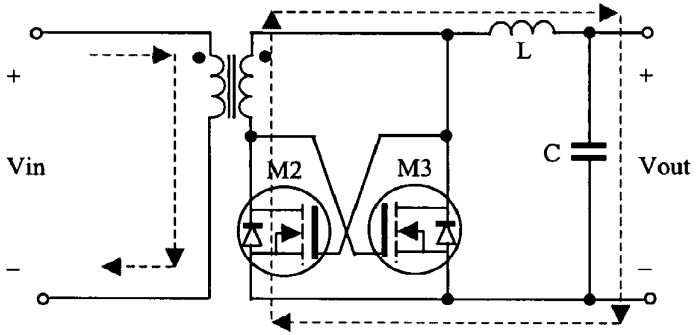


Self-driven synchronous rectification
isolated forward converter



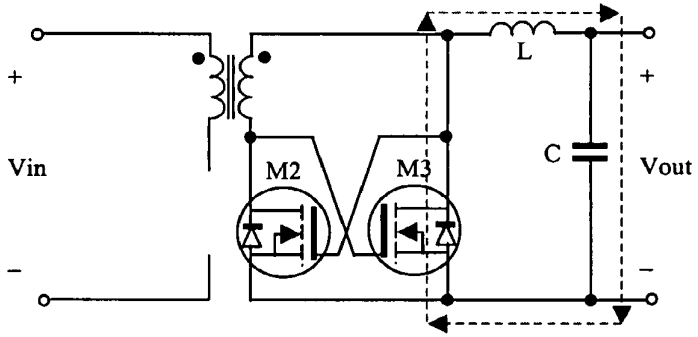
IC-driven synchronous rectification
isolated forward converter

Figure 2



Conduction mode (when M1 is ON)
equivalent circuit and current flow

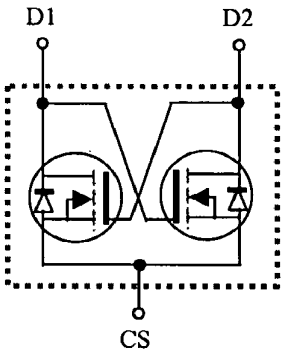
Figure 2a



Off mode (when M1 is OFF)
equivalent circuit and current flow

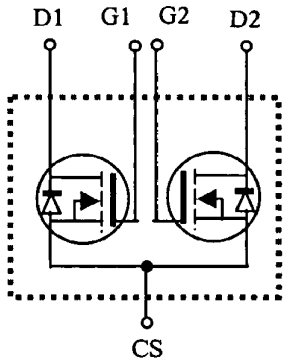
Figure 2b

Figure 3



First embodiment:
3-lead self-driven
synchronous rectification
MOSFET pair

Figure 3a



Second embodiment:
5-lead control IC-driven
synchronous rectification
MOSFET pair

Figure 3b

Figure 4

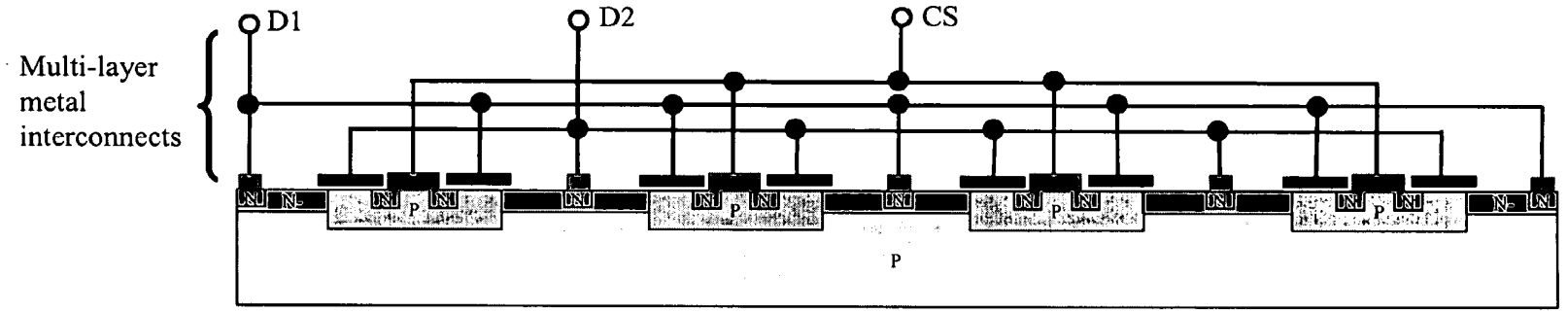


Figure 4a: First embodiment: 3-lead self-driven MOSFET pair in interleaved cell fingers

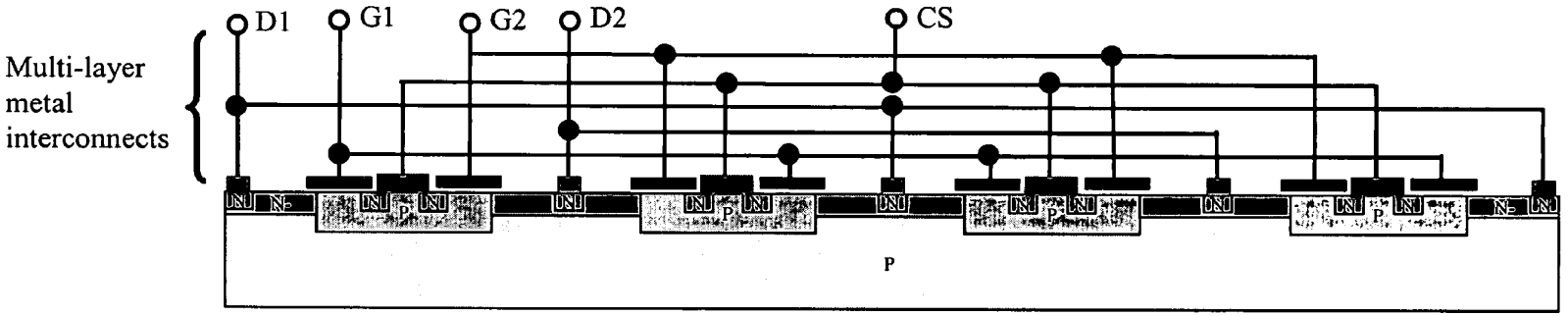


Figure 4b: Second embodiment: 5-lead external-driven MOSFET pair in interleaved cell fingers

Figure 5

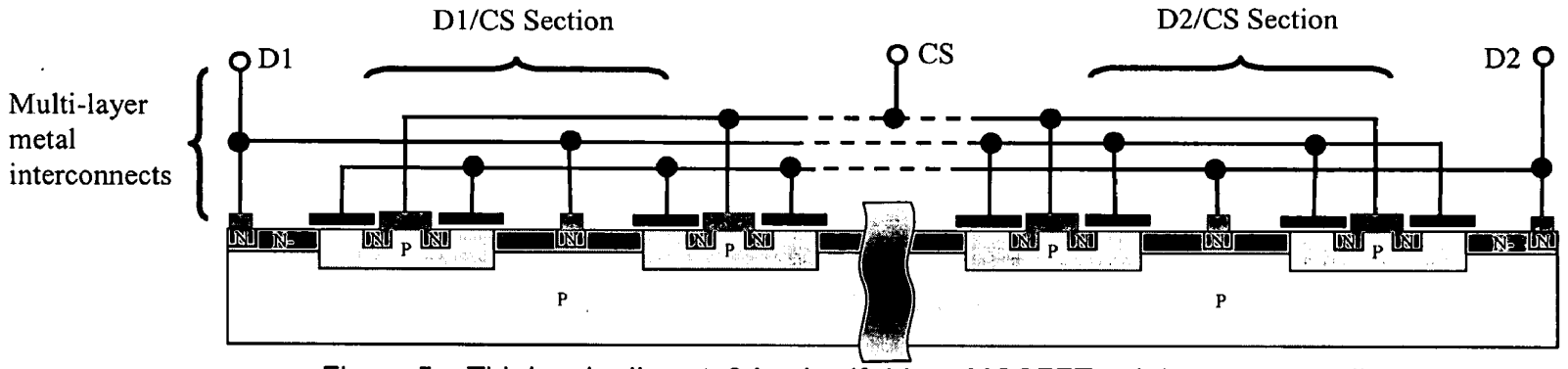


Figure 5a: Third embodiment: 3-lead self-driven MOSFET pair in separate cell sections

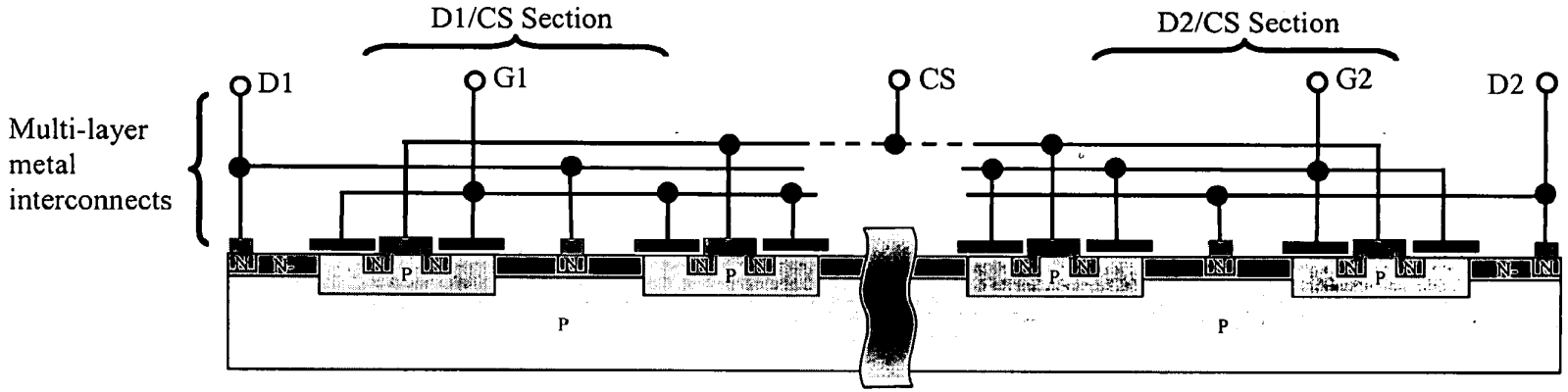
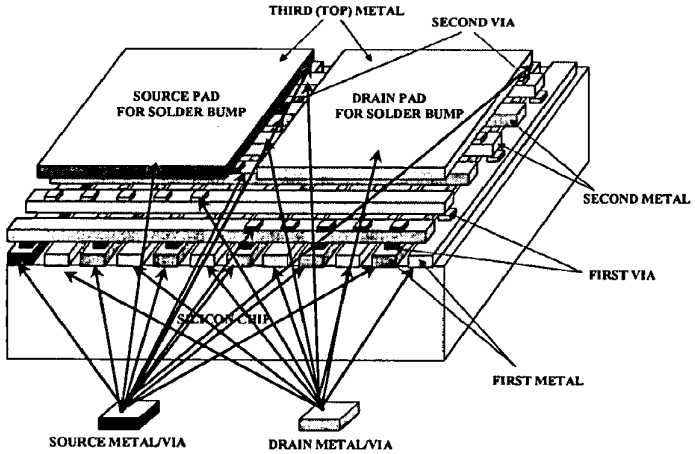
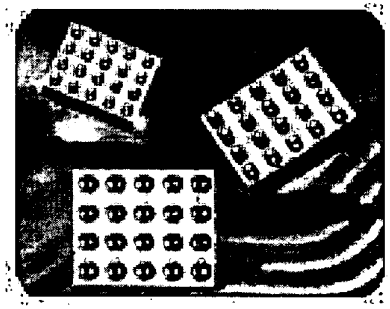
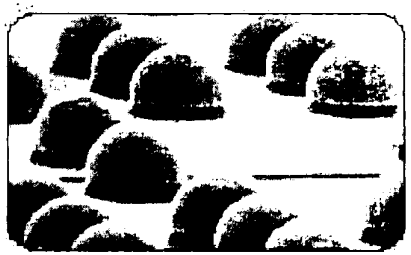


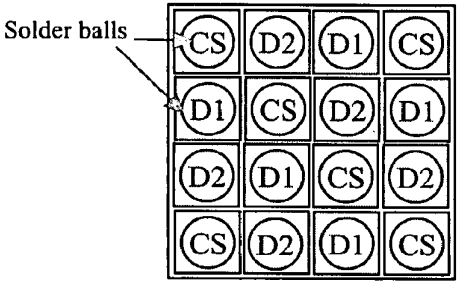
Figure 5b: Fourth embodiment: 5-lead external-driven MOSFET pair in separate cell sections

Figure 6

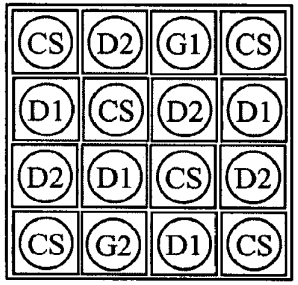




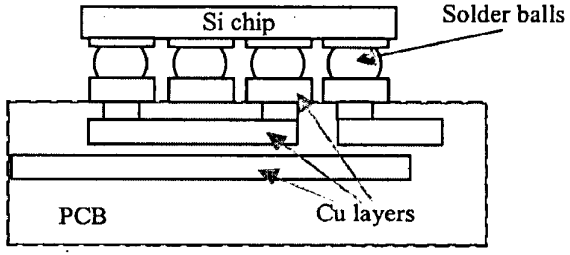




Top view of 3-lead embodiment



Top view of 3-lead embodiment



Cross-sectional view

Figure 7

- Potential Applications: Synqor, Power-One, Datel, etc.
- Prior Art Products: IR, Siliconix, STM ,Microsemi, etc.
- Comparison to IR's DirectFETTM IRF6603 (mainly targeted for synchronous rectification DC/DC converter applications)

	Chip Size (mm^2)	Rdson @4.5V (mΩ)	Qg @4.5V (nC)	Parts Count
IRF6603 DirectFET	3.9x5.5	3.9	48	2
GWS SyncMate	4.6x4.6	4.3	18	1